CLAIMS

1. In combination in a monolithic integrated circuit chip,

a plurality of repetitive cells each having a first branch responsive to a digital input voltage and having a second branch responsive to an individual one of progressive fractions of a reference voltage to provide an output signal representative of any difference between the input voltage and the individual one of the progressive fractions of the reference voltage,

an impedance network comprising a first set of impedance elements each connected to the first branches of first individual pairs of successive ones of the repetitive cells and a second set of impedance elements each connected to the second branches of second individual pairs of the successive ones of the repetitive cells,

the first set of the impedance elements defining a first impedance strip on the chip and the second set of the impedance elements defining a second impedance strip on the chip, and

each of the impedance elements in the first set being connected to repetitive cells which are responsive to progressive fractions of the reference voltage, such progressive fractions representing voltage differences between the successive cells connected to such impedance elements greater than the voltage difference between successive ones of the progressive fractions of the reference voltage,

each of the impedance elements in the second set being connected to repetitive cells which are responsive to the progressive fractions of the reference voltage, such progressive fractions representing voltage differences between the successive cells connected to such impedance element greater

than the voltage difference between successive ones of the progressive fractions of the reference voltage.